

# 1.5V 1:10 HSTL Fanout Buffer

## Features

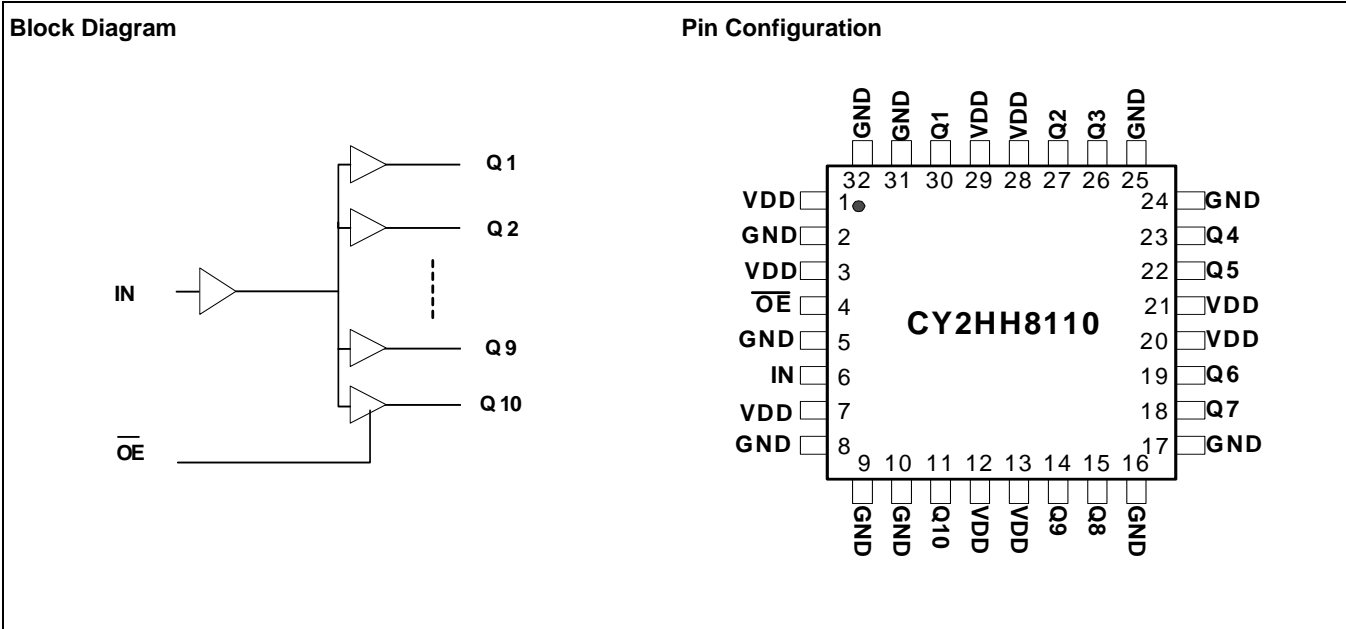
- DC to 150-MHz operation
- 1.5V power supply
- One single-ended HSTL input
- Ten single-ended Class II HSTL outputs
- Less than 1.9% Duty Cycle distortion
- Balanced 16-mA output drive
- Output Enable/Disable
- Low output-output skew
- Operating temperature range: 0°C to +85°C
- 32-pin TQFP package

## Description

The CY2HH8110 is a low-voltage HSTL fanout buffer designed for data communications, clock management, and specialty memory applications.

The class II HSTL outputs are balanced Push-Pull in design capable of delivering 16 mA into 10 pF load. This class allows both source series termination and symmetrically double parallel termination.

The CY2HH8110 low-output duty cycle distortion makes it suitable for Double Data Rate (DDR) applications.



**Pin Description<sup>[1]</sup>**

Pin	Name	I/O	Type	Description
6	IN	I	HSTL	<b>HSTL reference clock input</b>
30, 27, 26, 23, 22, 19, 18, 15, 14, 11	Q(1:10)	O	HSTL	<b>HSTL clock outputs</b>
4	OE	I, PD	LVC MOS	<b>Output enable/disable input.</b> When held LOW, outputs are enabled. When set HIGH, all outputs are disabled LOW.
1, 3, 7, 12, 13, 20, 21, 28, 29	VDD	Supply	VDD	<b>1.5V power supply<sup>[2]</sup></b>
2, 5, 8, 9, 10, 16, 17, 24, 25, 31, 32	GND	Supply	Ground	<b>Common ground</b>

**Notes:**

1. PD = Internal pull down.
2. A 0.1-uF bypass capacitor should be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the trace.

**Absolute Maximum Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD</sub>	DC Supply Voltage		-0.5	2.5	V
V <sub>DD</sub>	DC Operating Voltage	Functional	1.35	1.65	V
V <sub>IN</sub>	DC Input Voltage	Relative to V <sub>SS</sub> , with or V <sub>DD</sub> applied	-0.5	V <sub>DD</sub> + 0.5	V
V <sub>OUT</sub>	DC Output Voltage	Relative to V <sub>SS</sub>	-0.5	V <sub>DD</sub> + 0.5	V
V <sub>TT</sub>	Output termination Voltage			V <sub>DD</sub> ÷ 2	V
LU	Latch Up Immunity	Functional	200		mA
R <sub>PS</sub>	Power Supply Ripple	Ripple Frequency < 100 kHz		150	mVp-p
T <sub>S</sub>	Temperature, Storage	Non-functional	-65	+150	°C
T <sub>A</sub>	Temperature, Operating Ambient	Functional	0	+85	°C
T <sub>J</sub>	Temperature, Junction	Functional		+150	°C
∅ <sub>JC</sub>	Dissipation, Junction to Case	Functional		42	°C/W
∅ <sub>JA</sub>	Dissipation, Junction to Ambient	Functional		105	°C/W
ESD <sub>H</sub>	ESD Protection (Human Body Model)		1600		V
FIT	Failure in Time	Manufacturing test		10	ppm

**Multiple Supplies:** The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

**DC Electrical Specifications** (V<sub>DD</sub> = 1.5V ± 8%, T<sub>A</sub> = 0°C to +85°C)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
V <sub>IL</sub>	Input Voltage, Low	HSTL input, V <sub>REF</sub> = 0.75V	-0.30	-	0.65	V
V <sub>IH</sub>	Input Voltage, High		0.85	-	1.80	V
V <sub>IL</sub>	Input Voltage, Low	OE# input	-0.30	-	0.3 * V <sub>DD</sub>	V
V <sub>IH</sub>	Input Voltage, High		0.7 * V <sub>DD</sub>	-	V <sub>DD</sub> + 0.3	V
V <sub>OL</sub>	Output Voltage, Low <sup>[3]</sup>	I <sub>OL</sub> = 16 mA	-0.3	-	0.4	V
V <sub>OH</sub>	Output Voltage, High <sup>[3]</sup>	I <sub>OH</sub> = -16 mA	1.0	-	V <sub>DD</sub> + 0.3	V
I <sub>IL</sub>	Input Current, Low <sup>[4]</sup>	V <sub>IL</sub> = V <sub>SS</sub>	-	-	-10	μA
I <sub>IH</sub>	Input Current, High <sup>[4]</sup>	V <sub>IH</sub> = V <sub>DD</sub>	-	-	100	μA
I <sub>DDQ</sub>	Quiescent Supply Current	V <sub>IN</sub> = 0V, outputs disabled	-	-	1	mA
I <sub>DD</sub>	Dynamic Supply Current	Outputs loaded @ 62.5 MHz	-	215	250	mA
C <sub>IN</sub>	Input Pin Capacitance		-	-	6	pF
C <sub>OUT</sub>	Output Pin Capacitance		-	4.5	6	pF
Z <sub>OUT</sub>	Output Impedance		-	25	-	Ω

**AC Electrical Specifications** (V<sub>DD</sub> = 1.5V ± 8%, T<sub>A</sub> = 0°C to +85°C) <sup>[5]</sup>

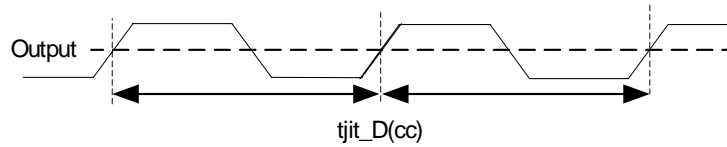
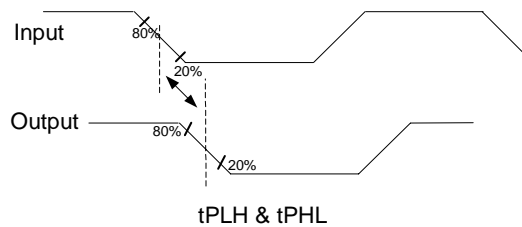
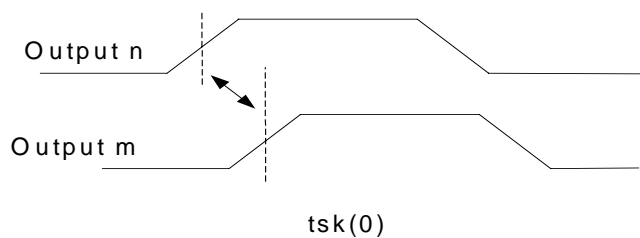
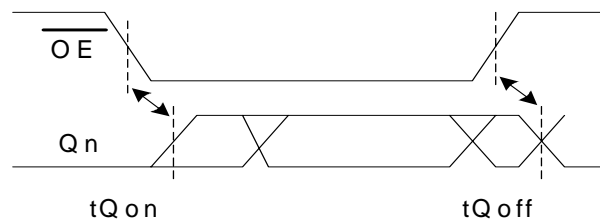
Parameter	Description	Condition	Min.	Typ.	Max.	Unit
f <sub>in</sub>	Input Frequency		-	-	150	MHz
V <sub>IL(AC)</sub>	AC Input HIGH Voltage	V <sub>REF</sub> = V <sub>DD</sub> /2, Internal Voltage Reference	0.95	-		V
V <sub>IH(AC)</sub>	AC Input LOW Voltage		-	-	0.55	V
t <sub>r</sub> , t <sub>f</sub>	Output rise/fall time <sup>[6]</sup>	20% to 80%	0.3	-	1.5	ns
DC	Output duty cycle	F <sub>out</sub> < 100 MHz	48	-	52	%
		F <sub>out</sub> > 100 MHz	45	-	55	

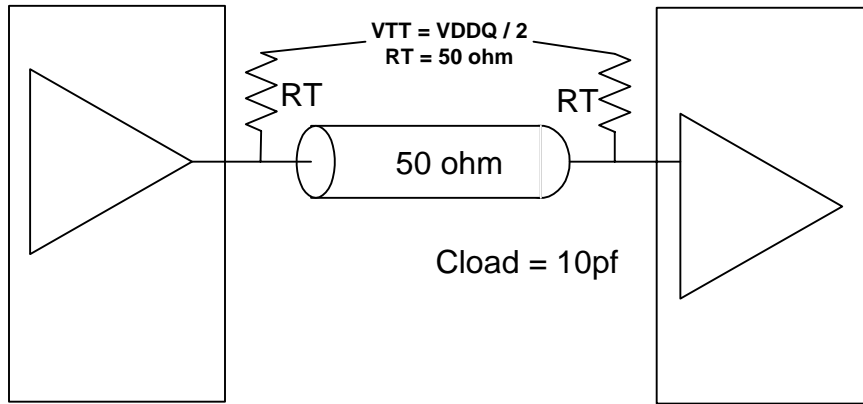
**Notes:**

- Driving 50Ω series terminated or symmetrically double parallel terminated transmission line to a termination voltage of V<sub>TT</sub>.
- Inputs have pull-down resistors that affect the input current.
- AC characteristics apply for series or parallel output termination to V<sub>TT</sub>. Parameters are guaranteed by characterization and are not 100% tested.
- t<sub>r</sub>/t<sub>f</sub> times are faster with parallel terminated loads.

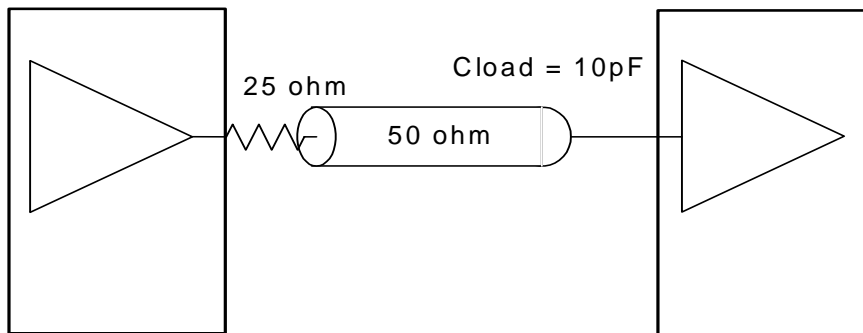
**AC Electrical Specifications** ( $V_{DD} = 1.5V \pm 8\%$ ,  $T_A = 0^\circ C$  to  $+85^\circ C$ ) (continued)<sup>[5]</sup>

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
tjit_DCD	Output Duty Cycle Distortion	Measure Jitter delay between input and output at $V_{DD}/2$ @ $f_{REF} = 62.5$ MHz	–	–	300	ps
		DCD @ $f_{REF} = 62.5$ MHz	–	–	1.9	%
t <sub>sk(O)</sub>	Output-to-Output Skew		–	–	200	ps
t <sub>sk(pp)</sub>	Part-to-Part Skew		–	–	2	ns
t <sub>PLH</sub>	Propagation Delay, Low to High		–	–	7	ns
t <sub>PHL</sub>	Propagation Delay, High to Low		–	–	7	ns
t <sub>Qoff</sub>	Output Disable Time		–	–	7	ns
t <sub>Qon</sub>	Output Enable Time		–	–	7	ns
t <sub>JIT(CC)</sub>	Cycle-to-Cycle Jitter, Deterministic jitter		–	10	50	ps

**Parameter Measurement Information**

**Figure 1. Cycle-to-Cycle Jitter**

**Figure 2. Propagation Delay from Input Reference to Output *n***

**Figure 3. Output to Output Skew**

**Figure 4. Output Enable/Disable Time**



**Figure 5. An Example HSTL Symmetrically Double Parallel Terminated Output Load | and CLASS II HSTL AC Test Load<sup>[7,8]</sup>**



**Figure 6. An Example HSTL Source Series Terminated Output Load<sup>[7,8]</sup>**

### Ordering Information

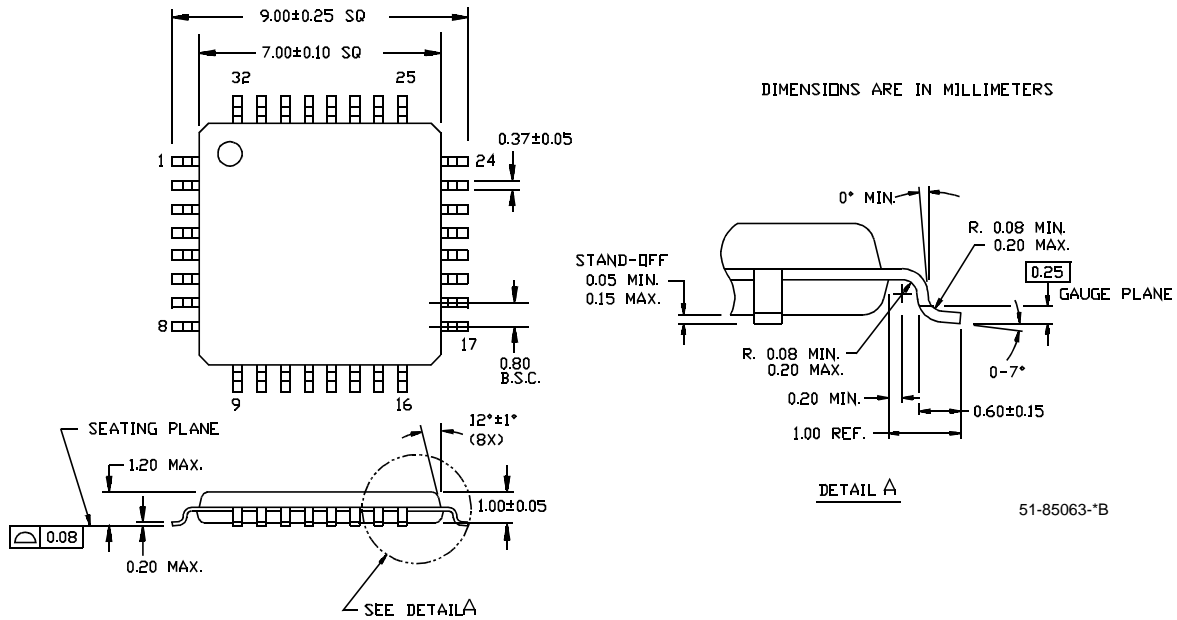
Part Number	Package Type	Product Flow
CY2HH8110AC	32-pin TQFP	Commercial, 0°C to +85°C
CY2HH8110ACT	32-pin TQFP – Tape and Reel	

**Notes:**

- 7. HSTL to HSTL input.
- 8. Cload includes probe and test board capacitance.

Package Drawing and Dimensions

32-Lead Thin Plastic Quad Flatpack 7 x 7 x 1.0mm A32



All product and company names mentioned in this document are the trademarks of their respective holders.

**Document History Page**

<b>Document Title:CY2HH8110 1.5V 1:10 HSTL Fanout Buffer</b> <b>Document Number: 38-07556</b>				
<b>REV.</b>	<b>ECN No.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	128398	08/04/03	RGL	New Data Sheet